LISTING OF CLAIMS

1. (Currently amended) A method of manufacturing a semiconductor memory device, the method comprising the steps of:

forming a charge trapping layer over a substrate;

forming a patterned hard mask layer over the charge trapping layer;

forming doped regions of a first conductivity type in the substrate by implanting ion species through the charge trapping layer using the hard mask layer to define an implant pattern of the doped regions;

laterally diffusing the doped regions into the substrate; and

forming buried bitlines of a second conductivity type in the doped regions and the substrate by implanting ion species through the charge trapping layer using the hard mask layer to define an implant pattern of the bitlines so that the forming and diffusing steps result in laterally diffused doped regions adjacent each buried bitline that inhibit ~~resulting in a doped region forming adjacent to at least one of the buried bitlines, wherein the doped region adjacent the at least one of the buried bitlines inhibits~~ a leakage current between adjacent pairs of ~~the~~ buried bitlines through substrate regions disposed between the diffused doped regions.

2. (Original) The method according to claim 1, further including the step of:

defining at least two regions in the charge trapping layer for programming and erasing the semiconductor device.

3. (Original) The method according to claim 1, further including the step of:

forming a conductive layer over the charge trapping layer,

wherein the charge trapping layer is interposed between the substrate and the conductive layer.

4. (Currently amended) The method according to claim 1, wherein the charge trapping layer is part of a multi-layer dielectric layer.

5. (Currently amended) The method according to claim 4, wherein the multi-layer dielectric layer includes a charge trapping dielectric layer as the charge trapping layer.

6. (Original) The method according to claim 5, wherein the multi-layer dielectric layer is an oxide-nitride-oxide (ONO) layer.

7. (Currently amended) The method according to claim 1, wherein the charge trapping layer is a ~~includes: a tunneling layer;~~ a charge trapping dielectric layer disposed over a ~~; and an insulating layer; wherein the~~ tunneling layer and disposed under an ~~is disposed over the substrate, the charge trapping dielectric layer is disposed over the tunneling layer and the~~ insulating layer ~~is disposed over the charge trapping dielectric layer~~.

8. (Original) The method according to claim 7, wherein a material of the tunneling layer is one or more of a SiO_2 or an oxynitride.

9. (Original) The method according to claim 8, wherein the charge trapping layer includes one or more materials of a permittivity greater than SiO_2.

10. (Currently amended) The method according to claim 9, wherein the one or more materials of the charge trappling layer are one or more of, silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), zirconium silicate, hafnium silicate, lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$,

$BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), or PMN ($PbMg_xNb_{1-x}O_3$) ~~or the like~~.

11. (Currently amended) The method according to claim 1, wherein the ~~further including the steps of: forming a~~ hard mask layer is patterned by ~~over the charge trapping layer;~~ depositing and patterning a photoresist layer over the hard mask layer to form a pattern in the photoresist; and transferring the pattern from the photoresist to the hard mask layer.

12. (Currently amended) The method according to claim ~~11~~ 1, wherein the first conductivity type is P-type ~~dopant type is boron~~ and the second conductivity type is N-type ~~dopant type is arsenic~~.

13. (Canceled)

14. (Currently amended) The method according to claim ~~13~~ 1, further including the steps of:

forming an insulating layer ~~over the hard mask layer, and planarizing the insulating layer such that the insulating layer~~ that fills apertures in the hard mask layer.

15. (Original) The method according to claim 14, further including the step of:

removing the hard mask layer.

16. (Currently amended) The method according to claim ~~11~~ 1, further including the step of:

annealing the semiconductor device to repair damage in the charge trapping layer due to the implanting of the ions to form the doped regions ~~first dopant type~~.

17. (Original) The method according to claim 1, wherein the charge trapping layer is a conducting layer.

18. (Original) The method according to claim 1, further including the step of:

forming a control gate over the charge trapping layer.

19. (Original) The method according to claim 18, further including the step of:

forming a multi-layer dielectric layer over the charge trapping layer,

wherein the multi-layer dielectric layer is interposed between the charge trapping layer and the control gate.

20. (Canceled)

21. (New) The method according to claim 1, wherein forming the buried bitlines damages the charge trapping layer and the method further comprises forming a conductive wordline over the charge trapping layer that does not have substantial coupling to the damaged portions of the charge trapping layer.